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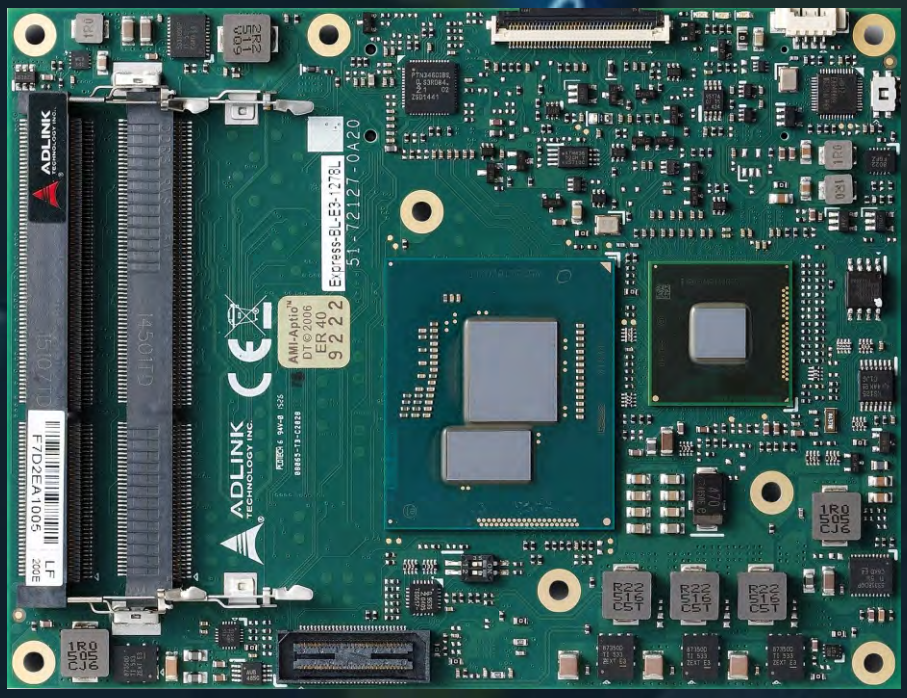
COM Express

New processor aims to deliver best price/performance ever



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"Did You Know?"

"A single Laser Peening shot generates 1 gigawatt of power for a 20 nanosecond time period…the same level of power generated continuously by a nuclear power plant."

Courtesy Curtiss-Wright

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ADLINK Launches First "Quad" Core™ i3 Value Processor on COM Express®

New processor aims to deliver **best price/performance ever**, benefiting mainstream high volume applications

27-Sep-2018

ADLINK, a leading global provider of advanced embedded modules, announces the addition of the quad-core Intel® Core™ i3-8100H processor to its recently released Express-CF COM Express Basic size Type 6 module based on the 8th Generation Intel® Core™ i5/i7 and Xeon® processors (formerly Coffee Lake).

Whereas previous generations Intel® Core™ i3 processors supported only dual cores with 3MB cache, the Intel® Core™ i3-8100H is the first in its class to support 4 CPU cores with 6MB of cache. This major upgrade results in a more than 80% performance boost in MIPS (million instructions per second), and an almost doubling of memory/caching bandwidth, all at no significant cost increase compared to earlier generations.

Intel® Core™ i3 processors are widely recognized as the best valued processor and are therefore preferred in high-volume, cost-sensitive applications. They are popular choices in gaming, medical and industrial control to name a few.

The ADLINK Express-CF-i3-8100H is currently in production.

Please contact ADLINK regional sales for samples

For more information about ADLINK Express-CF-i3-8100H, please visit:
https://www.adlinktech.com/Products/Computer_on_Modules/COMExpressType6/Express-CF_CFE?lang=en

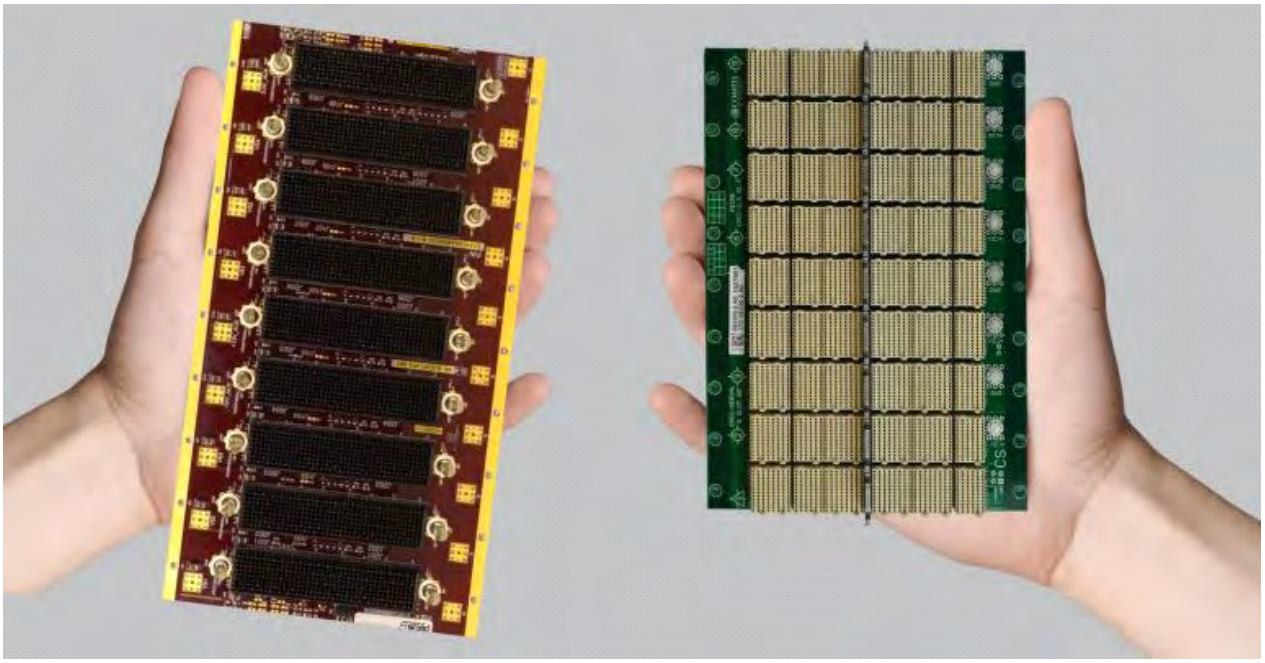
All Contacts Worldwide:
https://www.adlinktech.com/en/contactus.aspx

What's the Difference Between CompactPCI Serial and OpenVPX?

When upgrading computing systems, designers may be stuck deciding between the well-known OpenVPX or up-and-coming cPCI Serial for their next architecture. Are there mitigating factors that make one a slam dunk over the other?

Justin Moll | Sep 21, 2018

As legacy computing projects upgrade from VME and CompactPCI systems, or as new projects arise, an important choice is presented: "which direction do we go?" For open standard embedded computing, the technologies have advanced from bus-based platforms to high-speed serial architectures.



For VME, created by VITA, the follow-on generation architecture is OpenVPX using a completely different connector and routing system. For CompactPCI, created by PICMG, the follow-on generation architecture is CompactPCI Serial (cPCI Serial). It also has a new connector and routing approach. So, whether a user's legacy platform was VME or CompactPCI, it's completely open going forward in terms of selecting the next-generation architecture. For example, a previous VME user can select cPCI Serial for their upgrade path.

Similarities
So, what's the difference between cPCI Serial and OpenVPX? Let's start with their similarities. They both utilize the 3U and 6U × 160-mm-deep Eurocard form factor for the modules.

They're both excellent high-performance architectures available in air- or conduction-cooled formats. They utilize a 4HP (0.8 in.) slot pitch, but it's far more common for OpenVPX to use 5HP (1.0 in.) pitch even in air-cooled systems. For conduction-cooled modules, both specifications usually incorporate the 1.0-in. pitch spacing.
The two standards have routing provision for high-speed serial traffic such as PCIe Gen3 or 10GbE/40GbE (40GbE isn't yet specifically defined in these specifications). There are also control planes, expansion planes, utility planes, and provisions for SAS/SATA, clocking, and more. Therefore, both architectures can be utilized for a wide range of high-performance data processing, signal conversion, digitizing, and multicore communication across a backplane-based system. Furthermore, both architectures can be employed in commercial/industrial-grade as well as rugged/Mil-grade applications.

The differences are primarily the high-performance serial connector used, interoperability, slot availability and I/O, power options, ecosystem availability, and price. OpenVPX utilizes the MultiGig RT series connector, while cPCI serial opts for the Airmax VS series.
In addition, VPX was initially less defined (under VITA 46), leading to some interoperability issues. The VITA group later created OpenVPX (under VITA 65) with defined pinout libraries called "profiles" to help overcome the concerns. cPCI Serial defines a simple topology structure for different slot configurations, ensuring interoperability. The advantage of the OpenVPX approach is there's more flexibility in routing configurations. The potential downside is the complexity in maintaining interoperability between slot, module, and backplane pinout profiles.

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Rugged Versions

Where VME was applied in a wide range of markets, OpenVPX is primarily used in defense applications. This is a mainly a price issue, as the industrial, medical, and several other markets are more price-sensitive. Because cPCI Serial is designed to be a relatively low cost for the level of performance, the architecture is used in markets that include, but aren't limited to, industrial automation, railway, communications, medical, and defense. cPCI Serial is beginning to see increased usage in defense applications. There are a wealth of ruggedized and conduction-cooled options and even a RAD-hard variant called cPCI Serial Space.

A board vendor and a backplane/chassis vendor both recently entered the North America-based market, and a large U.S. defense program recently selected cPCI Serial. OpenVPX is highly successful in Mil/Aero applications and its ecosystem in those programs is diverse.

Multicore Processing

Both OpenVPX and cPCI Serial can provide multicore, multiprocessor communication across the slots. OpenVPX has the advantage of having very-high-power options (up to 768 W theoretically), allowing for the use of fast (and hot) processors. 3U cPCI Serial has up to 80 W of power for each slot and 171 W for the 6U version. However, a double-wide module (8HP) or greater can be used to leverage more pins for higher power requirements.

The power-rail options for 3U OpenVPX are +3.3 V, +5 V, +12 V, −12 V, 3.3 V AUX, and 48 V. They provide the advantage of flexibility, but the disadvantage of having to provide PSUs that support multiple rails. This significantly increases the costs, especially for pluggable units. Conversely, 3U cPCI Serial only uses 12 V (with a +5-V standby option). The approach is less versatile, but it's cost-effective and simple. The 6U version also allows the use of −48 V.

Another cost-effective dimension of cPCI Serial is its high-performance serial connector is much lower cost, despite offering near apples-to-apples performance. Overall, it's expected that most cPCI Serial systems are as low as half the cost of OpenVPX. Ethernet is the primary interface for multiprocessing for cPCI Serial and the P6 connector is dedicated for a (typical) mesh interface.

I/O Availability, Slots, and Hot Swap

The cPCI Serial topology is primarily a star configuration (one hub going to each payload slot) for the fat pipes; a full x4 PCIe interface would be limited to nine slots (one hub and eight payload). A full mesh (all slots directly interconnected) is also possible in smaller paths. Moreover, it's possible to have, for example, a 17-slot system/backplane, where slots 2-9 have no SATA and slots 10-17 have SATA only. Such types of configurations could be used for storage racks (8x Hard Disk Drives), but they're not defined in the specification.

Figure 1 shows an example of a 5-slot 3U cPCI Serial chassis. As the slot counts are typically lower, the chassis used is 42HP wide (9.5 in.). This is half the width of a standard 84HP (19 in.) rackmount chassis.

1. This example of a cPCI Serial chassis from Pixus Technologies demonstrates the commonly compact width of the high-performance open-standard computing architecture.

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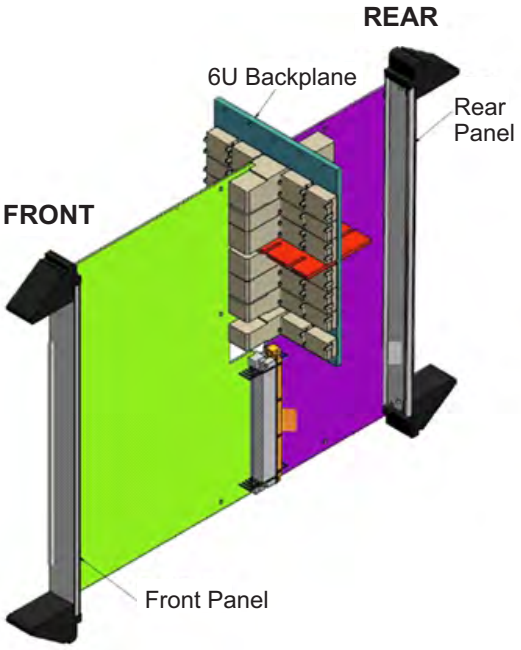
OpenVPX provides lots of flexibility in connections that are double fat pipe (x8) or fat pipe (x4), thin pipe (x2), ultra-thin pipe (x1), etc. How these connections are utilized in each configuration is determined by the VITA 65 profile. One can certainly utilize these types of connections in cPCI Serial, but they're not specifically defined in the specification. This would also allow, for example, a x2 configuration in cPCI Serial to go beyond nine slots. Alternatively, customized versions can utilize undefined I/O for enough pins to expand x4 PCIe in more slots. It should be noted that these versions would not necessarily comply with the specification, and interoperability with standard-compliant modules could be jeopardized.

OpenVPX and cPCI Serial provide a wealth of I/O pins, depending on the configuration and several factors. The use of rear I/O is interesting in cPCI Serial. The connectors on the front of the backplane aren't populated in several locations to reserve them for rear I/O. If rear I/O is required, then the connectors are populated on both the front and the rear. A standard 3U cPCI Serial backplane has 224 rear I/O pins available on slot 2 and 3, and 240 pins available on slots 5 through 9. The potential benefit is that the connectors aren't populated unless needed; thus, money is saved.

Conversely, in OpenVPX, the front connectors are often all used for various signals. So, the front connectors are typically all present, whether rear I/O is needed or not. If rear I/O is required, then the connectors are populated in the rear of the backplane as needed.

The 6U option for cPCI Serial is also interesting. It provides a separate rear connector interface to an rear transition module (RTM). This approach allows the 3U portion of the backplane to be fully utilized while providing dedicated pins to a separate rear board. It's similar to the approach of other PICMG specifications such as AdvancedTCA and MicroTCA.4. Figure 2 (left) shows the dedicated pin area for the rear I/O and Figure 2 (right) shows the 6U board interface. Alternatively, a 6U RTM in OpenVPX would plug directly into the RTM connectors in the same slot (and plane) on the backplane as the front boards.



2. cPCI Serial only populates certain front connectors if rear I/O is required, otherwise they're left blank (left). For additional I/O, the 6U cPCI Serial form factor has a rear module interface (right). (Image on left courtesy of Schroff)

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As its predecessor CompactPCI allowed, cPCI Serial facilitates hot-swappability, where all FRUs (including the board modules) can be removed or inserted while the system is still running. OpenVPX doesn't facilitate hot-swap of the board modules.

Ecosystem

The ecosystem of the architecture constitutes the number of board, chassis, and specialty product vendors that support the technology. cPCI Serial has at least eight board vendors (and growing) and at least five chassis vendors. As cPCI Serial is adopted in more defense applications, it's expected that more U.S.-based vendors will enter the market.

Since OpenVPX has been around longer and is extremely successful in defense applications, it has a vast ecosystem to support that market. More and more cPCI Serial vendors are developing high-end FPGAs and multi-core processors. When the technology develops a larger footprint in defense, one could image that more boards will be developed for analog-to-digital and digital-to-analog, or versions that accept front mezzanine cards (FMCs) with various sample rates and channel options to be utilized.

Two Successful Technologies

Both OpenVPX and CompactPCI Serial are excellent high-performance architectures. OpenVPX has tremendous brand recognition, particularly in the Mil/Aero arena. The cPCI Serial architecture is growing in adoption in the U.S. and its brand is gathering more steam globally. OpenVPX has a wide ecosystem/deployment and technically seems to have advantages in high-power, high-slot-count systems.

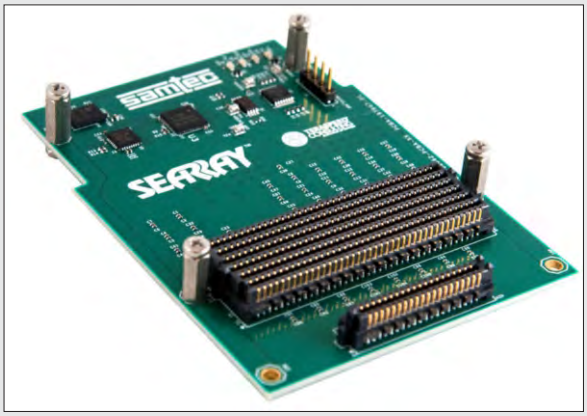
For mid-sized to small systems or ATR applications, the architectures seem to have comparable performance. cPCI Serial would likely have a significant advantage in price. OpenVPX would hold a big advantage in being well-known in the industry. Overall, users should know that multiple architecture options are available for commercial, industrial, & military high-performance embedded computing systems. END

ANSI and VITA Ratify ANSI/VITA 57.4-2018 FPGA Mezzanine Card Plus (FMC+) Standard

Tuesday, July 24, 2018 11:13 AM | Jerry Gipper (Administrator)

Increased throughput to 28 Gbps

VITA, September 27, 2018 — VITA, the trade association for standard computing architectures serving critical and intelligent embedded computing systems markets, announces the ratification by ANSI and VITA of ANSI/VITA 57.4-2018 "FPGA Mezzanine Card Plus (FMC+) Standard". This standard has completed the VITA and ANSI processes reaching full recognition under guidance of VITA. The FMC+ standard extends the Gigabit transceiver support specified in ANSI/VITA 57.1 by adding two new connectors that enable additional Gigabit transceivers running at higher data rates.



FMC+ adds an optional extension connector (the High Serial Pin Connector extension, or HSPCe) to boost pin-count by 80 positions, arranged in a 4 X 20 array. This brings the maximum multigigabit interfaces to 32 full duplex channels. Additionally, throughput per multigigabit interface has increased to 28 Gbps in each direction. This will allow for higher data rates and expanded bandwidth to all fit within the same form factor as FMC.

Additional signals to support backplane reference clock and synchronization have been added. The ANSI/VITA 57.4 standard defines functionality to maintain backward compatibility between new VITA 57.4 carrier cards and existing VITA 57.1 mezzanine modules.

"Samtec is proud to offer the next-generation FMC+ connector solution" said David Givens, VITA 57.4 working group chair and Standards Director at Samtec. "The customized SEARAY™ has flawless reliability. It provides extensive flexibility to FPGA developers and VITA-hardware users alike, while maintaining ideal signal integrity." The SEARAY connector technology is key to meeting the data transfer goals established by the VITA 57.4 working group.

Copies of the standard are available for purchase at the VITA Online Store.

About VITA

Founded in 1984, VITA is an incorporated, non-profit organization of suppliers and users who share a common market interest in critical embedded systems. VITA champions open system architectures. Its activities are international in scope, technical, promotional, and user-centric. VITA aims to increase total market size for its members, expand market exposure for suppliers, and deliver timely technical information. VITA has American National Standards Institute (ANSI) and International Electrotechnical Commission (IEC) accreditation to develop standards (VME, VXS, VPX, OpenVPX, VPX REDI, XMC, FMC, FMC+, VNX, Reliability Community, etc.) for embedded systems used in a myriad of critical applications and harsh environments.
For more information, visit www.VITA.com.

Esterline CMC Electronics and Green Hills Software Join Forces at AUSA 2018

Companies Demonstrate Green Hills INTEGRITY-178-tuMP Operating System Running on CMC's Next Generation Display

Washington D.C. — Oct. 8, 2018 — Esterline is pleased to announce that its next generation CMC Electronics MFD-3068 smart display will be featured in the Green Hills Software booth no. 9053 at this year's AUSA show (Association of the U.S. Army). The display will be operating with the Green Hills Software INTEGRITY®-178 tuMP™ Multicore operating system.

Esterline's third-generation MFD-3068 smart display is designed as an open architecture platform, featuring next-generation MOSArt™ (Modular Open System Architecture) middleware developed to non-proprietary industry standards for the partitioning of applications (ARINC 653) and for high assurance operating systems like the Green Hills INTEGRITY-178 tuMP Multicore operating system.

Esterline CMC Electronics' initial deployment of INTEGRITY-178 tuMP on the MFD-3068 was for Airbus Helicopters' CH-53GS/GE Sea Stallion Upgrade, Patria's Grob 115E Upgrade for the Finnish Air Force and with several undisclosed programs also under contract. INTEGRITY-178 tuMP has since become the first operating system certified as conforming to the FACE Technical Standard for Intel Multicore Processors.

"Today's multicore technology offers significant flexibility in meeting the processing throughput required for our advanced line of smart displays and mission computers," said Marc Bouliane, Product Director, Avionics Display Solutions, Esterline. "Our goal is to achieve the ideal Size, Weight, and Power reduction (SWaP) by leveraging modern multicore parts while simultaneously harnessing as much of their available capacity as possible. Green Hills is a supplier capable of meeting these SWaP and throughput goals without jeopardizing our safety certification requirements. After a very thorough and extensive trade study, Green Hills Software's INTEGRITY-178 tuMP was the only RTOS that met all of these requirements."

With an optical quality second to none, the MFD-3068 offers true 8-bit color rendition with optical performance stabilized over its design life-time and its extended operating temperature envelope (+70C continuous). Its next-generation Light Emitting Diode (LED) illumination system supports multi-mode operations day/night/NVIS) and provides up to 275 fL of illumination in day mode. This display solution with Green Hills INTEGRITY-178 tuMP and Esterline's MOSArt™ Middleware allows customers to host their own applications (Patria), host applications from Esterline (Airbus Helicopters) and 3rd parties, or any combination, providing significant flexibility in meeting customer needs.

About Green Hills Software www.ghs.com

Founded in 1982, Green Hills Software is the worldwide leader in embedded safety and security. In 2008, the Green Hills INTEGRITY-178 RTOS was the first and only operating system to be certified by NIAP (National Information Assurance Partnership comprised of NSA & NIST) to EAL 6+, High Robustness, the highest level of security ever achieved for any software.

About Esterline Corporation http://esterline.com/

Esterline Corporation is a leading worldwide supplier to the aerospace and defense industry specializing in three core areas: Advanced Materials; Avionics & Controls; and Sensors & Systems. With annual sales of approximately $2 billion, Esterline employs roughly 13,000 people worldwide.

Alstom certifies a Kontron 3U VPX computer at the SIL-4 level for safe railway applications

Augsburg, Germany / Toulon, France, July 17, 2018 – Kontron, a leading global provider of IoT/Embedded Computing Technology (ECT), today announced that its COTS 3U VPX-based embedded computer has successfully been qualified and certified at the higher security level SIL-4 by Alstom for safe railway applications.

"We are very pleased to have been selected by Alstom, a worldwide leading supplier of reliable and safe transportation systems, to provide our COTS-based safety embedded computers," said Alain Spors, Director of Sales at Kontron. "The Kontron offering meets the high level of quality and performance required by Alstom."

The Safe Computing Unit 'SCU' computer consists in extractable Line Replacement Units (LRU) in order to provide a low maintenance time and repair (MTTR). Both the ventilation drawers and the electronic cards are easily extractable. The computing unit of the SCU featuring single board computers (SBCs) and an ethernet switch card takes advantage of the versatility and modularity of a 3U VITA 46 VPX standard architecture to offer a SIL-4 certifiable and long-term maintainable solution.

Thanks to its ISO / TS 22163 (formerly IRIS) certification, Kontron provides Alstom with a high level of design, production, testability, and traceability to meet the requirements of the railway sector.

Nicolas Catheland, Program Manager at Alstom, said: "The qualification of the SCU for our new railway signaling programs confirms Kontron's ability to meet the high standards of quality we expect, whether for products or long-term service delivery."

For more information please visit:
https://www.kontron.com/industries/transportation

UTC Expects to Close Rockwell Collins Acquisition by October

By Woodrow Bellamy III, Avionics International | September 20, 2018

United Technologies Corporation (UTC) CEO Greg Hayes admits that his company's $30 billion acquisition of Rockwell Collins is taking longer than expected, but the company should officially finish the acquisition process by the end of this month.

Hayes said during the Morgan Stanley Laguna Conference last week that he expected the acquisition to have been completed by now.

"If you would've asked me three months ago, I would've said almost any day," he said. "The fact is it has taken us a little bit longer. We still expect to close before the end of this month."

The chief executive feels the two companies have addressed "all of the questions from the regulatory agencies." He also explained that one of the reasons it's taken longer than expected results from difficulty in finding a buyer for one of the businesses operated by Rockwell Collins. That has been resolved, though, after French aerospace and defense manufacturer Safran signed an agreement to acquire the flight controls and electric actuators product line Rockwell Collins previously owned.

Safran's acquisition is subject to regulatory approval, although according to a statement released in Safran's earnings results from the first half of 2018, the company expects to close that acquisition within the first six months of 2019.

Under UTC's acquisition, Rockwell Collins will become a combined business unit with UTC Aerospace Systems (UTAS) called "Collins Aerospace Systems." Rockwell Collins CEO Kelly Ortberg will lead the combined Collins Aerospace business and UTAS President Dave Gitlin will become its COO.

The combination of the aerospace systems division of UTC and the Rockwell Collins' avionics manufacturing, defense business and interiors unit — the latter from Rockwell Collins' 2016 acquisition of B/E Aerospace — provides opportunities for many synergies, especially in terms of new aircraft technologies and concepts that the two companies can explore.

As an example, Rockwell Collins supplies the cockpit displays on the Boeing 737 MAX, 777X and 787. The company is also well known for continually expanding the capabilities of its Pro Line Fusion avionics flight deck.

UTAS is well known for providing aircraft interface device (AID) technology and has continually expanded and improved upon its aircraft health monitoring offerings in recent years. Both companies have also provided other avionics offerings outside of AIDs and displays such as aircraft connectivity and radar systems.

Emirates, for example, is in the process of upgrading its 777 fleet with virtual quick-access recorder technology from UTAS. Meanwhile, Rockwell Collins just announced a new contract from the U.S. Air Force to provide its fleet of KC-135s with a real-time information in the cockpit system.

Hayes told the Morgan Stanley audience he believes the acquisition of Rockwell Collins "looks a heck of a lot better than it did 12 months ago" and that the company has already identified at least $500 million in cost synergies. The only short-term concern expressed by Hayes about the acquisition is the performance of the B/E interiors unit.

"If you think specifically about the Collins business, they would tell you the base avionics business, the defense business, has done better than what we have forecast a year ago, where we have seen some concern is in the interiors business. This is the legacy B/E business. They're a little bit, not surprisingly, behind plan," said Hayes.

Curtiss-Wright, Green Hills Software and CoreAVI Collaborate to Deliver FACE™-Aligned, DO-254/178 Safety-Certifiable Solutions

Support for Green Hills Software's INTEGRITY®-178 tuMP™ RTOS and CoreAVI's graphics drivers on Curtiss-Wright rugged modules speeds the integration of high-performance avionics systems

October 31, 2018 | BY: John Wranovics

Ashburn, Va. – October 31, 2018 -- Curtiss-Wright's Defense Solutions division today announced that it has collaborated with Green Hills Software and Core Avionics & Industrial Inc. (CoreAVI) to deliver industry-leading FACE™-aligned, DO-254/DO-178 safety-certifiable high-performance graphics and computing solutions for avionics applications. Curtiss-Wright's rugged VPX3-152 single board computer (SBC), VPX3-719 graphics and video capture module, and VPX3-611 I/O module, combined with Green Hills' INTEGRITY-178 tuMP multi-core real time operating system (RTOS) and CoreAVI's suite of high-performance OpenGL® ES/SC drivers and EASA ED-12C/ FAA DO-178C Level A certification packages enable system designers building avionics system for aerospace, military and other high reliability markets to easily and rapidly integrate complete rugged DO-254/DO-178 safety-certifiable system.

"We are excited to continue our successful collaboration with Green Hills and CoreAVI to bring industry-leading DO-254 and DO-178C safety-certifiable processing and graphics solutions to the avionics market," said Lynn Bamford, Senior Vice President and General Manager, Defense Solutions division. "When combined with the INTEGRITY-178 RTOS and CoreAVI's graphics drivers, our SBCs, graphics modules and I/O cards provide system designers with the critical building blocks they need to quickly and cost-effectively develop safety-certifiable systems."

About Green Hills Software INTEGRITY-178 tuMP RTOS

The INTEGRITY-178 tuMP RTOS is the only operating system (OS) certified to conform to the FACE Technical Standard for both the Safety Base and Security Profiles for the C, C++ and Ada programming languages. INTEGRITY-178 tuMP remains to date the only FACE conformant OS that offers true multicore processing with concurrent operation across all the cores. The RTOS has successfully met the DO-178 DAL A certification objectives multiple times, across several different multicore SOC architectures, each of which featured a different core design. The INTEGRITY-178 tuMP RTOS is available for all of Curtiss-Wright's DO-254 safety-certifiable products, including its SBCs featuring Power Architecture®, Intel®, and Arm® processors. (www.ghs.com).

Last month, at the 2018 U.S. Army FACE Technical Interchange Meeting (TIM), Curtiss-Wright, in collaboration with Harris Corporation and Green Hills, publicly demonstrated the first working example of a FACE-conformant OS and FACE-conformant software application running simultaneously on two completely different processor infrastructures (Intel and NXP® Power Architecture).

About the VPX3-152 Single Board Computer

Curtiss-Wright's VPX3-152 is a DO-254 DAL A safety-certifiable, commercial SBC. The rugged 3U OpenVPX™ module features NXP's QorIQ® T2080 multicore SOC. For safety-certifiable SBC designs, the QorIQ T2080, a quad-core AltiVec™-equipped 64-bit Power Architecture SOC processor, has emerged as a de facto standard thanks to its support from a wide range of field-proven OS vendors, such as Green Hills. Curtiss-Wright designed the 3U VPX VPX3-152 from the ground up to be cost-effective and support DO-254 DAL A safety certifiability for critical defense and aerospace avionics applications. The VPX3-152 takes full advantage of the T2080's features to reduce the chip count and complexity, which lowers the cost and the risk associated with the safety certification effort. Designed for use in size, weight, and power (SWaP)-constrained applications, the VPX3-152's compact 3U design is ideal for use in a wide range of C4ISR applications deployed in harsh environments, especially those that require safety-certifiable DO-254 hardware and DO-178C software.

About the XMC-719 Graphics Card

Curtiss-Wright's DO-254 safety certifiable XMC-719 graphics module features built-in HD-SDI video capture and output interfaces. It supports extremely low latency video capture, graphics generation and overlay, with flexible I/O interfaces. The card's AMD E8860 Radeon™ GPU is supported with up to six independent and simultaneous graphics outputs selectable from 4x DVI, 2x HD-SDI, and 2x analog RGBHV or STANAG interfaces. The VPX3-719 provides 2 GB of dedicated video memory, and a hardware accelerated video compression encoder and decoder. It features built-in video capture and format conversion and provides two channels of video capture from HD-SDI, analog RGBHV, or STANAG sources. The video data is transferred directly to processor or GPU memory. Curtiss-Wright also offers the VPX3-717 DO-254 safety-certifiable graphics module for applications which do not need video capture.

Curtiss-Wright, Green Hills Software and CoreAVI Collaborate to Deliver FACE™-Aligned, DO-254/178 Safety-Certifiable Solutions

About CoreAVI Safety Critical Software Drivers

CoreAVI provides the industry's leading safety critical graphics, video and compute drivers which enable integrators of safety critical embedded systems to maximize the performance of the latest graphics and compute technology. CoreAVI's FACE-aligned graphics drivers are developed from the ground up to optimize performance and maximize reliability. All CoreAVI products are available with COTS certification evidence to support the certification of systems to the most stringent levels of RTCA DO-254/DO-178C and EUROCAE ED-80/ED-12C. (www.coreavi.com).

About the VPX3-611 Safety Certifiable I/O Module

Curtiss-Wright's VPX3-611 is an FPGA-based rugged 3U VPX module that can be configured with a virtually unlimited combination of DO-254 / DO-178 safety-certifiable I/O interfaces. Because DO-254 certification artifacts are available for the module's I/O interfaces at the FPGA block macro-level, I/O configuration variants of the VPX3-611 can be created quickly and at minimal cost compared to the development of a custom solution. Safety-certifiable I/O interfaces supported by the VPX3-611 include MIL-STD-1553B, ARINC 429, CANbus, asynchronous UARTS, discretes, analog in, analog out, Serial Peripheral Interface (SPI), and others (contact factory for additional information).
For more information about Curtiss-Wright's Defense Solutions division, please visit www.curtisswrightds.com.

About Curtiss-Wright Corporation

Curtiss-Wright Corporation is a global innovative company that delivers highly engineered, critical function products and services to the commercial, industrial, defense and energy markets. Building on the heritage of Glenn Curtiss and the Wright brothers, Curtiss-Wright has a long tradition of providing reliable solutions through trusted customer relationships. The company employs approximately 8,600 people worldwide. For more information, visit www.curtisswright.com.

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John Wranovics has over thirty years experience in the management of media relations and the promotion of high technology products. He has been with Curtiss-Wright since 2003. He has a degree in English Literature from the University of California, Berkeley.

Wind River Announces Formation of Board of Directors

Leading Industry Executives Designated to Oversee Strategic Direction of Newly Independent Software Company

ALAMEDA, CA – September 19, 2018 – Wind River®, a leader in delivering IoT software to critical infrastructure, today announced the formation of a Board of Directors and a Board Advisor designation. The appointments follow Wind River's recent acquisition by TPG Capital from Intel.

The board and advisor members will provide perspective and guidance on the ongoing strategic direction of Wind River. They will also play an important role in helping the company as it works with customers to accelerate the evolution from automated devices to autonomous systems across a diverse range of use cases.

Each member is highly distinguished and brings extensive and proven executive management and technology expertise to help Wind River, representing key areas of the company's business. The inaugural appointments joining Wind River President and Chief Executive Officer Jim Douglas include the following individuals: Moshe Gavrielov (Executive Chairman), Afshin Mohebbi, Nehal Raj, Art Heidrich and Mark Fields (Board Advisor).

Moshe Gavrielov (Executive Chairman) served as president and CEO at Xilinx, Inc., where he drove the company through a broad strategic and operational transformation resulting in a significant market cap expansion approaching a valuation of $20B. Prior to Xilinx, he served as executive vice president and general manager of the verification division at Cadence Design Systems. Before that, he was CEO of Verisity, Ltd., where he drove the company's emergence from a small private entity, through a successful NASDAQ IPO, delivering ongoing profitable top and bottom-line growth leading to the eventual acquisition by Cadence for $315M.

Press Release Source:Wind River

About Wind River

Wind River is a global leader in delivering software for the Internet of Things. The company's technology has been powering the safest, most secure devices in world since 1981, and is found in more than 2 billion products. Wind River offers a comprehensive edge-to-cloud portfolio, supported by world-class global professional services and support and a broad partner ecosystem. Wind River software and expertise are accelerating digital transformation of critical infrastructure systems that demand the highest levels of safety, security, performance, and reliability.
To learn more, visit Wind River at www.windriver.com.

Embedded Computing Boards Overview

Direct Link Click on the Pictures

Qseven

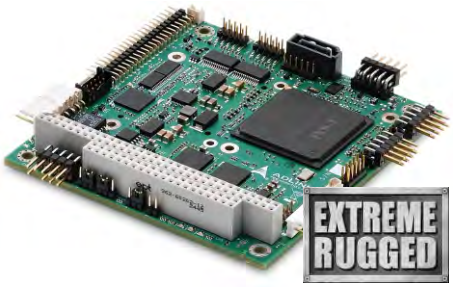
Intel-based: several CPU 's
Standard Size (70 mm x 70 mm)

SMARC

Smart **M**obility **ARC**hitecture

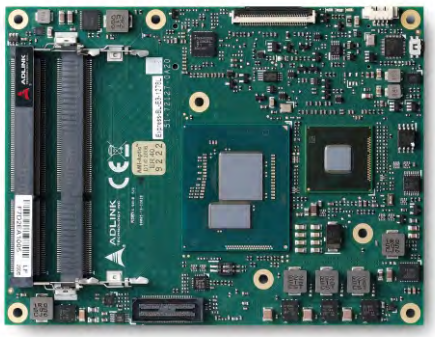
Intel-based: several CPU 's
Short Size (82 mm x 50 mm)
Full Size (82 mm x 80 mm)

PC/104
PCI/104 Express



Intel-based: several CPU 's
PCI/104-Express (V3.0)
Size (117.4 mm x 96 mm)

COM Express



Intel-based: several CPU 's

Type 6
Basic Size (125 x 95 mm)
Compact (95 x 95 mm)
Type 7 - Intel Xeon-based
Basic Size (125 x 95 mm)
Type 10
Mini Size (84 x 55 mm)
Type 2
Basic Size (125 x 95 mm)
Compact (95 x 95 mm)

3U-6U VPX

Conduction & Air-cooled

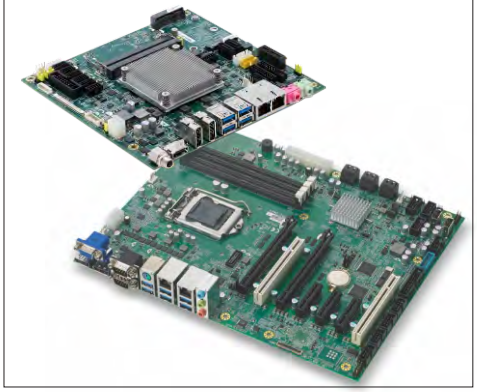
3U-6U CompacPCI, Plus & Serial

Conduction & Air-cooled

AdvancedTCA - ATCA -AMC - MicroTCA

ADLINK vigorously promotes the advantages of the ATCA technology by providing complete platform solutions that offer high-density processing power, faster data throughput, and intelligent system management. Designed for next-generation telecom, datacom, and equipment manufacturers, ADLINK's ATCA platforms significantly reduce over-all development costs, come with extended operating lifecycles, and speed up critical time-to-market.

Ind. Motherboards Mini-ITX



PCIe

Frame Grabbers
Video Capture Cards

PXI - PXIe

Auto Chip Design, Test Changes Ahead

Which tools and methodologies will work best to ensure electronics operate for extended periods of time under harsh conditions?

September 19th, 2018 - By: Kevin Fogarty, Technology editor at Semiconductor Engineering

The automotive industry's unceasing demand for performance, coupled with larger and more complex processors, are driving broad changes in how electronics are designed, verified and tested.

What's changing is that these systems, which include AI-oriented logic developed at the most advanced process nodes, need to last several times longer than traditional IT and consumer devices, and they need to work under conditions that even a year ago would have been considered unrealistic. This is forcing changes from one end of the supply chain to the other, raising questions about how this will impact time to market, cost, and which approaches ultimately will work best.

"The automotive and functional safety requirements in ISO 26262 are a whole different paradigm of chip development than we did before," said Bryan Ramirez, strategic marketing manager at Mentor, a Siemens Business. "You have to give a different level of assurance that, your product can recover and operate normally, even if there is a particle from space or some other random event—or that it will fail safely. And you have to define what that safe failure is."

This is the basis of ISO 26262 and advanced driver-assistance systems, which are aimed at increasing safety in autonomous and semi-autonomous vehicles.

"ADAS systems represent the most severe requirements for reliability, and they have to survive 15 years or more to meet requirements for electronic components of autonomous vehicles," according to Norman Chang, chief technologist at ANSYS. "That's a lot different than 2.5 years for mobile. There are issues with aging, NBTI and electromigration, which can be thermal-related. You can also see degradation in performance. It usually takes a lot of time to totally break down, but performance can be reduced along the way."

Which approaches will work best under these conditions aren't clear at this point, however. For one thing, much of this technology is brand new. There is no history to show how a 7nm logic chip will behave under extreme environmental conditions over a period of years. That means reliability needs to be simulated, defects and potential defects need to be discovered with various flavors of verification, and test strategies need to be developed early enough in the design process to make sure nothing falls through the cracks.

"Adding heat and durability to existing design/test flows increases the time required and the cost," according to Anil Bhalla, senior manager of marketing and sales at Astronics Test Systems. "The automotive test flow is a function of complexity. Where do you want to test? Either there is more focus on system-level test, or you look at what you can shift around in the flow and what you want to catch that can cause failures. If you're characterizing a device for -40° to 150°C, most of your effort is around qualification, not production. So do you do that in the flow, or move some to final test, or can some of that happen in wafer-level test?"

More time and more cost comes from the need to verify SoCs or components that may include the latest 7nm node sizes working in concert with components built on a host of other nodes, sometimes several generations older, Bhalla said.

Increasingly, OEMs and Tier-1 suppliers are demanding that automotive electronics have zero faults, which goes well beyond making sure that nothing is broken. It means a chip or module or system won't do anything that will make a vehicle unsafe, even when something random and unexpected happens.

"You have to build in the ability to self-correct or fail safely," said Derek Floyd, director of business development for Advantest. "You will need to validate the technology to get to level 5. That means power, analog, microcontrollers, sensors. You need to test LiDAR systems and safety sensors. And then you have to figure out which version you're using for which product. On top of that, with automotive you need two or three suppliers."

That complicates matters further, because various components from multiple vendors will behave differently under different operating conditions. Time is not always kind to chips or the systems in which they operate, but it's far less kind when a car is baking in the sun or exposed to sub-zero temperatures.

"You can't assume the part you create now will always operate correctly," said Mentor's Ramirez. "Silicon products will develop faults over time—whether it's just from aging or particles from space or whatever. One of the things you have to do is provide a Failure-in-Time (FIT) rate showing how often that kind of transistor fails (in a billion hours of operation). But what it means to fail could differ different depending on the [Automotive Safety Integrity Level] ASIL level. You might have elements that operate at ASIL A in one component and ASIL D in another, so the demand and the testing to prevent failure would be different and you have to take that into account. The last thing you want would be for a particle from space or something random to cause an airbag to go off in your face."

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The nightmare for both chip and automakers is the 2013 Toyota sudden-acceleration problem, which generated more than 6,000 complaints and crashes that resulted in 89 deaths. Toyota tried to settle in 2013 with a $3 million settlement after analysis showed software in a faulty electronic throttle control could open the throttle all the way, causing the car to accelerate more quickly than a driver could compensate for even applying the brakes with full force. The settlement ultimately cost Toyota $1.2 billion."

That's part of the need for documentation," Ramirez said. "It's all about if the OEM can provide proof that they did everything they were required to do."

Rearranging resources

Many companies making the leap into automotive have had to put a greater emphasis on verification and test, and they have been forced to rearrange resources, according to John Bongaarts, senior product manager for semiconductor test software at National Instruments.

"We've seen customers making a number of changes to functionalize verification," Bongaarts said. "In the past, a large company might have had disparate design centers producing individual components and having testing done separately by just one person on each team. Now we see functionalization and standardization of that testing that puts testing on a team that handles a broad portfolio of products. We've seen other adaptations, too—companies using ATE systems for verification at times, for example."

Jim Hogan, managing partner of Vista Ventures, LLC and a leading investor in EDA companies and technologies, calls the current era Verification 3.0—a stage defined by a hybrid of existing methodologies combining simulation, emulation and formal verification. Verification 1.0, according to Hogan, revolved around simulation running on individual workstations; Verification 2.0 added formal verification and emulation in discrete roles.

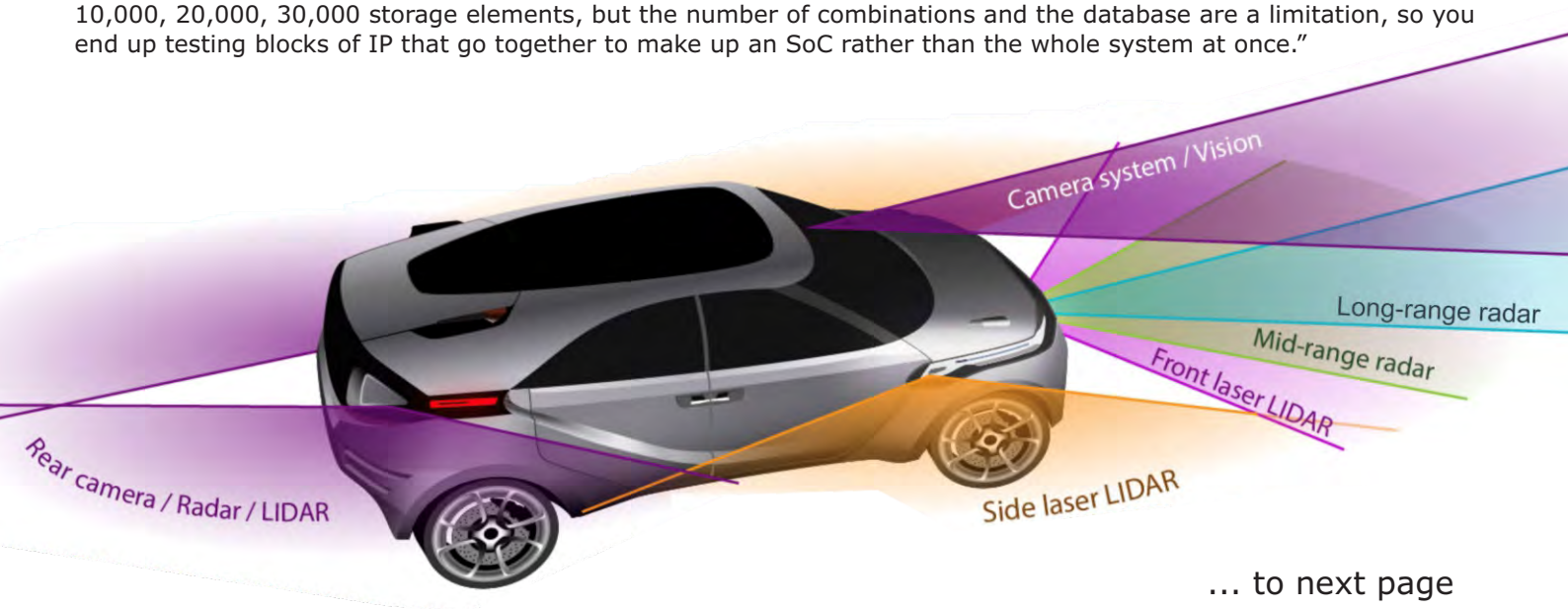
The elevated stakes are driving changes in the roles and priorities those methodologies, but the integration among tools to apply those methods and the efficiency of flow in applying them is still rough enough that the question of what Verification 3.0 will actually look like is still very much up in the air, Ramirez said.

More formal

The additional emphasis on formal verification makes sense, however due to the relative simplicity of translating the assertions that are critical to a formal verification's tests and the requirements of standards like ISO 26262, according to Dave Kelf, vice president of marketing for Breker Verification Systems.

It is also a good match for its ability to provide mathematical proof and documentation that a particular function is present and will work as expected, and its ability to examine all the requirements of a standard and compare them against every possible response from the specific block of IP it is verifying, Kelf said.

Formal creates a database of all the possible states this design can get into and all the ways to transition to the next state, on purpose or by some random occurrence. That's why it's so powerful for automotive—you can guarantee something won't happen without relying on exhaustive simulation or emulation testing, where you get a model to run through every scenario and watch to see what happens," Kelf said. "You can get up to testing a million gates, or 10,000, 20,000, 30,000 storage elements, but the number of combinations and the database are a limitation, so you end up testing blocks of IP that go together to make up an SoC rather than the whole system at once."



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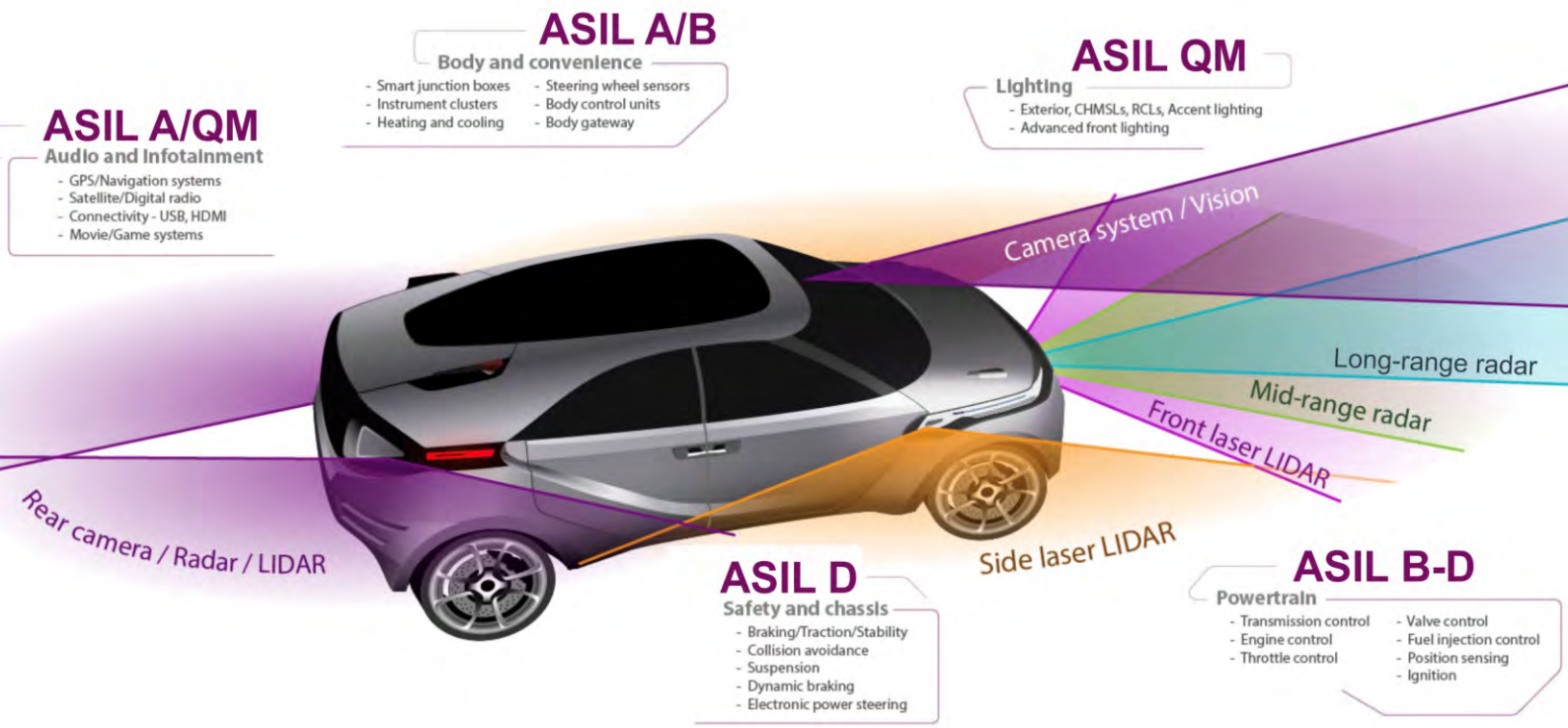

Fig. 1: ASIL levels and applications. Source: MIPS

Others agree, but with some caveats. "Formal lets you go through all the possible scenarios, so it can also help you get to 100% code coverage faster [than simulation], where you have to run through all these scenarios to collect the result," Ramirez said. "The challenge is how to scale it. You can break a product up into smaller hierarchical blocks and verify each individually, but these automotive chips are becoming bigger and more complex faster than formal is becoming more efficient."

There has been enough standardization of assertion formats and enough tools available to help convert requirements to assertions that the verification team don't have to write every bit of every set of assertions by hand using, according to Tom Anderson, technical marketing consultant at OneSpin Solutions.

What works best where

"It's a significant amount of work to have to build an alternate model of a design using assertions," Anderson said. "There's a great benefit in being able to test every possible state, but there's no question it's a lot of work. And you still have to verify a byte at a time. With simulation you can cover a much wider base, but you also risk missing a lot of the corner cases that might turn out to be important."

Simulation can cover a much wider part of a design than formal, but often uses more system resources due to the need to keep throwing new scenarios and possible faults at the model while hoping not to miss a corner case or special circumstance that could end up as a major fault, Anderson said.

Portable Stimulus and other high-level, abstracted approaches to defining assertions and translating requirements can make formal verification simpler, quicker and easier to manage, but not enough to counter the inherent, practical size limit on formal verification, Kelf said.

"You're creating a database with every state a chip can get into and then you're asking questions about that chip," Kelf said. "Doing that across an entire chip is basically impossible. Most verification that people do is still with simulation and emulation. Formal was mostly used for smaller, very specific purposes, but it's becoming more general-purpose."

Portable stimulus helps automate and scale the verification process by taking a high-level view of the whole process and creating models that allow requirements to be translated more easily into formats required by formal, simulation and emulation test processes, Kelf said.

A lack of integrated toolsets capable of managing all three methods has made progress more difficult, but test-equipment and software developers have been focused during the past year or two on integrating capabilities well enough to allow verification to become a flow applied several times during the development cycle, not just once at the end.

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In 2016, a Mentor-sponsored survey of verification methods and results showed that adoption of simulation-based methods including code coverage, assertions and functional coverage that had been growing quickly during the mid-2000s had flattened out, possibly due to the scaling limitations of simulation using these techniques the report suggested.

Use of automated formal applications—which had been considered very labor intensive when handled manually—grew 62% between 2012 and 2014; automated formal property checking grew 31% between 2014 and 2016, implying a shift toward formal verification but not at the cost of existing use of simulation.

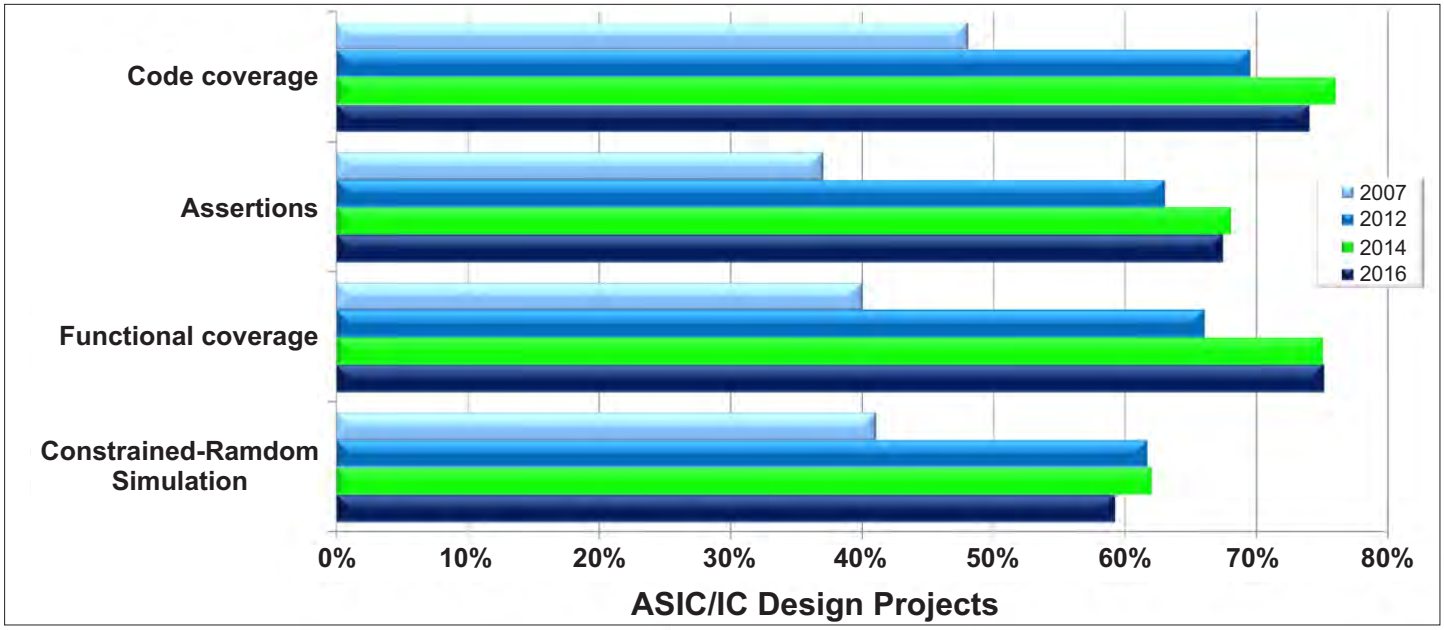

Fig. 2: ASIC/IC dynamic verification adoption trends. Source: Mentor, a Siemens Business

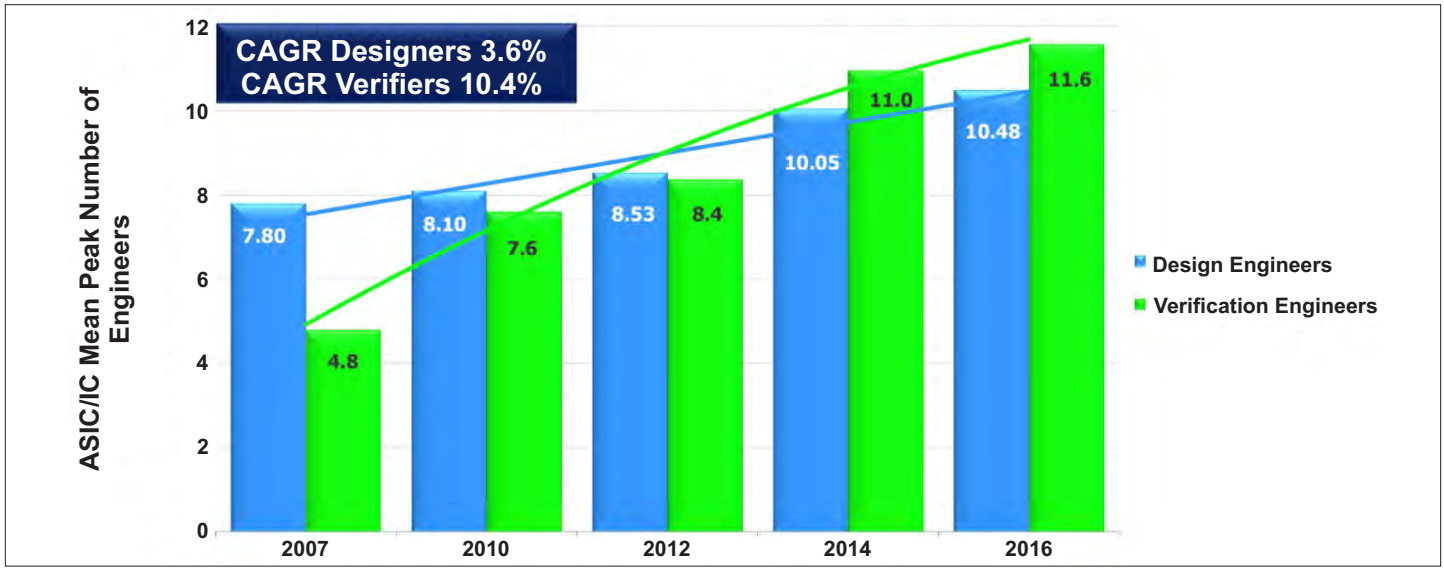

Fig. 3: Verification engineers vs. design engineers. Source: Mentor, a Siemens Business

It is likely adoption of those techniques will flatten, as well, as growth in complexity and size of the IC to be verified outpaces the growing maturity of the automatic formal verification products.

The study also shows the number of engineers working at verification growing at 10.4% while designers grew only 3.6%—indicating that, efficient or not, scalable or not, demand for verification continues to grow at a healthy pace.

Growth in demand is only one piece of the puzzle, however.

"The big problem is how do we get these solutions and methodologies to scale to fully address functional safety testing of big chips," Ramirez said. "The problems are being solved at the block level. Will they really ever work effectively with a 2-billion-gate ADAS chip? How do you address safety across the system, not just the chip? There are a lot of complexities that make it difficult to scale. I just don't see right now how they're going to accomplish that."

End